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Published in:
Analog Integrated Circuits and Signal Processing

Link to article, DOI:
10.1007/s10470-017-1012-5

Publication date:
2017

Document Version
Peer reviewed version

Noname manuscript No.
(will be inserted by the editor)

Fully Integrated, Low Drop-Out Linear Voltage Regulator in 180 nm CMOS

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Received: date / Accepted: date

Abstract This paper presents a capacitor-free low dropout (LDO) linear regulator based on a dual loop topology. The regulator utilizes two feedback loops to satisfy the challenges of hearing aid devices, which include fast transient performance and small voltage spikes under rapid load-current changes. The proposed design works without the need of a decoupling capacitor connected at the output and operates with a 0-100 pF capacitive load. The design has been taped out in a 0.18 µm CMOS process. The proposed regulator has a low component count, area of 0.012 mm^2 and is suitable for system-on-chip integration. It regulates the output voltage at 0.9 V from a 1.0 V - 1.4 V supply. The measured results for a current step load from 250-500 µA with a rise and fall time of 1.5 µs are an overshoot of 26 mV and undershoot of 26 mV with a settling time of 3.5 µs when C_L between 0-100 pF. The proposed LDO regulator consumes a quiescent current of only 10.5 µA. The design is suitable for application with a current step edge time of 1 ns while maintaining ΔV_{out} of 64 mV.

Keywords Linear Voltage Regulators · Low Drop-Out · Capacitor-free · Capacitor-less · Dual-Loop · Fast Transient Response

1 Introduction

Nowadays, linear voltage regulators are important components integrated circuits. For on chip power management, where multiple supply voltages are used, low drop-out (LDO) voltage regulators play an important role. Improving power management will help to extend the battery life and could increase the

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use of portable devices. As the industry is pushing towards complete system-on-chip (SoC) design solutions, including improving power management, LDO voltage regulators becoming a main factor. They are needed to provide voltage supplies for circuits with steep load transients and for protecting sensitive circuits from supply voltage disturbances. Their superior noise-ripple rejection over switching regulator makes them suitable to supply noise sensitive circuits. Linear regulators have some advantages over switch mode power supplies as they provide lower output noise, less electromagnetic emission, high power supply rejection ratio (PSRR) and are easy to integrate on-chip within a small area while maintaining an accurate output voltage.

In portable devices such as hearing aids, there is a strict requirement on area. The number of discrete components must be minimized, as the electronics must fit in the ear canal. Implementing a capacitor free LDO regulator will help to reduce the overall size by eliminating the large output decoupling capacitor and increase the reliability of the system. On the other hand, for a voltage regulator without an on-chip capacitor (usually referred as capacitor-free or capacitor-less) does not have a large capacitor to set the dominant pole and stable the circuit. In the application at hand the estimated capacitance of load circuitry is between 0-100 pF. The absence of an output capacitor rises issues in the transient response, ΔV_{out} (undershoot and overshoot) that will be larger and there will be an increase of the settling time. Moreover a large output capacitor ensures stability as it will set the dominant pole and acts as a supply for the frequency components of the current load, I_L, outside the bandwidth of the regulator.

Removing the external capacitor requires the circuit to overcome the transient response and stability issues mentioned. There have been a number of capacitor-free topologies suggested in the literature. This previous research mainly focus on improving the transient performance [1] - [4]. One approach is to use active feedback and slew-rate enhancement circuit [5]. Another approach is a LDO structure with a three-stage amplifier and damping-factor-control frequency compensation [1] or utilizing voltage spike detection [3]. Articles [13], [14] suggested an adaptive biasing technique, to increase the bias current according to the magnitude of I_L. All these approaches and others ([11] and [12]) result in a rather complex design, large area and normally high quiescent current.

Some voltage regulators use NMOS as pass device [15]. These designs can be smaller in size due to the higher charge carrier mobility in NMOS devices, thus enabling the same drain current with a smaller area. A PMOS pass element reduce the minimum required voltage drop across it. The advantage of using PMOS as pass transistor is that the supply voltage does not need to be significantly higher than the output voltage. Smaller voltage headroom results in less power dissipation, essential for devices like hearing aids.

Modern hearing aids need to fit in the ear canal, no integrated chip intended for such applications can be larger than 8-10 mm^2. Therefore each single block that goes into the design need to be as small as possible. Absolute area is crucial in hearing aids as it need to fit all the analog and digital circuits.

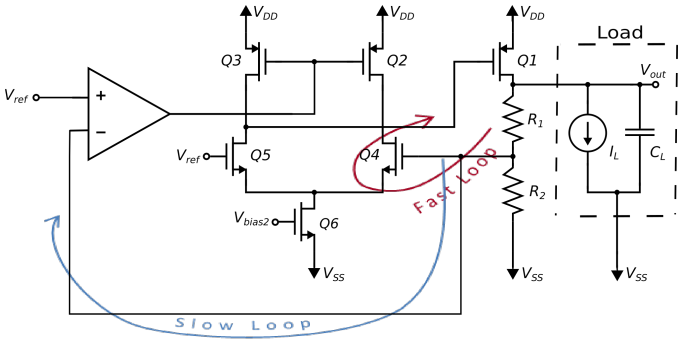

Fig. 1 Fast loop and slow loop of the proposed LDO linear voltage regulator

In this paper, Section II presents the circuit description and introduces the two regulation loops and its design details. Section III discusses the simulation results. Then, Section IV discusses the experimental results. Discussion of performance comparison with former work is presented in Section V. Finally, the conclusions of this paper are given.

This paper is an extended version of the work in [10] published in IEEE International Nordic Circuits and Systems Conference (NORCAS) in 2016.

2 Proposed Architecture and Circuit Description

The new design proposed in this work has two regulation loops similar to [7]. This design is a LDO using a PMOS pass transistor configured as a common source (CS) amplifier while [7] uses a NMOS as the pass transistor with a common drain stage. Refer to Fig. 1 for the circuit diagram of the proposed regulator. The design specifications target the following parameters. The regulator is supplied by nominal voltage of 1.2 V and outputs a voltage of 900 mV. The load current, I_L, is 250-500 µA which is stepped with a 1 ns rise and fall time[1]. The capacitance C_L represents the load of up to 100 pF.

The fast loop consists of a differential amplifier stage, driving the common source (CS) amplifier, which include the pass transistor (Q1). The PMOS transistors in the differential stage (Q2 and Q3) are controlled by the slow loop containing the operational amplifier. The proposed design does not contain any large passive devices and has a low count of transistors. The simplicity allows for easy and area efficient implementation, while demonstrating good performance. Moreover, reaching stability is simpler compared to other designs due to the low number of poles and zeros. The following sections describe the two control loops in detail. The circuit was biased from two different current sources for debugging purposes. The full circuit diagram can be found in Fig. 2.

[1] Edge time of 1.5 µs was used for measurements and compared to simulations due to measurement limitations

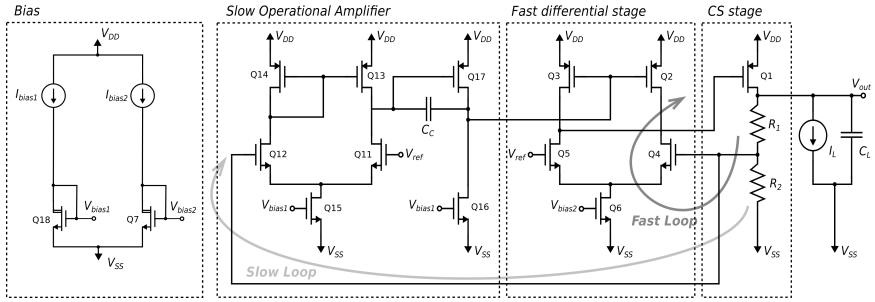

Fig. 2 Full schematic of the proposed LDO linear regulator

2.1 Principle of Operation of the Fast Loop

The fast loop directly regulates the gate of the pass transistor. Its purpose is to suppress the spikes in the output voltage, V_{out}, which is due to a step in the load. The overall performance of the regulator is impacted by the amplitude of the voltage spikes and the recovery time. By assuming the fast loop constitutes an underdamped system, the gain bandwidth product (GBWP) of the open loop gain will be inversely proportional to the settling time T_s. Therefore we will design the fast loop to have large GBWP. There is a trade-off between the circuit quiescent current in fast loop stage and the GBWP of the loop. As can be seen in Fig. 2, this loop starts at the gate of Q4 and ends at the drain of Q1.

The open loop transfer function, $A_{OL}(s)$, is described in (1). In order to analyze the loop, the equation was divided into two parts, CS stage $H_1(s)$ described in (2) and differential stage $H_2(s)$ described in (5). From the analysis of the transfer function it can be realized that the parasitic capacitance and resistance of the pass transistor (Q1) dominate the poles ω_{p1} (3) and ω_{pa} (6). The gate-source capacitance is C_{gs1} and C_{gd1} is the gate-drain capacitance of Q1. The output resistance is represented by r_{ds1} and g_{m1} is the transconductance of Q1. The analysis was done with a load capacitance C_L to understand its impact on the system, therefore in the zero load case $C_t = C_{gd1}$. In this work the maximum value of the load capacitance was 100 pF. The transfer function $H_1(s)$ has two poles ω_{p1} and ω_{p2}, both are depended on C_t, C_{gd1} and C_{gs1}. The dominant pole ω_{p1} denominator include also R_t and R_s. Moreover, the second pole is proportional to the transistors transconductance, having a large g_{m1} will push ω_{p2} to higher frequencies.

$$A_{OL}(s) = H_1(s)\ H_2(s)\ \frac{R_2}{R_1 + R_2} \tag{1}$$

$$H_1(s) = -g_{m1}R_t\ \frac{1}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{2}$$

$$\omega_{p1} \approx \frac{1}{C_t R_t + R_s(C_{gs1} + g_{m1}R_t C_{gd1})} \tag{3}$$

$$\omega_{p2} \approx \frac{g_{m1}C_{gd1}}{C_{gs1}C_{gd1} + C_{gs1}C_L + C_{gs1}C_L} \tag{4}$$

For (2) - (4), $R_t = r_{ds1} \| (R_1 + R_2)$, $C_t = C_L + C_{gd1}$, $R_s = r_{ds3} \| r_{ds5}$. From $H_2(s)$ transfer function, the dominant pole ω_{pa} is set by R_{diff} and C_{gd1}. The second pole ω_{pb} and zero ω_z denominators are C_g which is equal to the sum of C_{gs2} and C_{gs3} while both nominators are proportional to g_{m3}. The differential stage and common source stage set the gain of the fast loop. By maximizing g_{m1} we can achieve higher gain for the CS stage. The poles and zeros were selected in the design of the fast loop to achieve high GBWP. The high W/L ratio of Q1 will introduce a large gate capacitance and transconductance which on one hand, will dominate the frequency response of the fast loop. On the other hand, a large pass transistor will also cause high parasitic capacitances which will impact the regulator performance. This big capacitance will also push the non-dominate poles to lower frequencies and potentially closer together, and therefore at some point compromise the system stability.

$$H_2(s) = -g_{m5}R_{diff} \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{pa}})(1 + \frac{s}{\omega_{pb}})} \tag{5}$$

$$\omega_{pa} \approx \frac{1}{R_{diff}C_{gd1}} \tag{6}$$

$$\omega_{pb} \approx \frac{g_{m3}}{C_g} \tag{7}$$

$$\omega_z \approx \frac{2g_{m3}}{C_g} \tag{8}$$

Where, $C_g = C_{gs2} + C_{gs3}$, $R_{diff} = r_{ds3} \| r_{ds5}$. The resistors R_1 and R_2 are used to set the gate voltage of Q4 and keep the transistor in saturation. The feedback resistance network values is $R_1 = 300\ k\Omega$ and $R_2 = 600\ k\Omega$. The quiescent current in the differential stage of the fast loop, see Fig. 2, should be minimized to achieve overall low current consumption. By choosing the W/L ratio as mentioned for Q1, the output capacitance of this stage will mainly be the gate capacitance of Q1, C_{g1}, which will be larger than the capacitances of the other nodes. The gain of the differential stage in the fast loop is set primarily by the output resistance of transistors Q3 and Q5. Another aspect is the power supply rejection ratio which can be increased by using larger length for transistors Q2-Q5.

When current step loads are applied, ringing can occur on the output of the regulator due to low phase margin of the loop response. Therefore it is desirable to keep the fast loop phase margin above 75 degrees at maximum expected load capacitance.

2.2 Principle of Operation of the Slow Loop

The role of the slow loop is to control the gate voltage of transistors Q2 and Q3 and thereby stabilize the DC level at V_{out}. A two stage operational amplifier (OpAmp) with Miller capacitor compensation has been utilized for this function. The slow loop is designed to consume a low quiescent current and therefore will have low power consumption. Transistors Q11 to Q18 and the miller compensation capacitor constitute the OpAmp as can be seen in Fig. 2. The slow loop starts at the gate of Q12, then through the OpAmp, proceed from the gate to the drain of Q3 and then from the gate to the drain of Q1. In order not to degrade the frequency response of the fast loop, this OpAmp has a unity gain frequency approximately two decades below that of the fast loop. Therefore the dominate pole of the OpAmp was placed at a low frequency, at 100 Hz as can be seen in the OpAmp frequency response in Fig. 3. We use a large Miller capacitor to move the dominant pole to lower frequency without affecting the second pole. Moreover, the loop has to be stable to maintain the stable operation of the whole system.

When the steps in I_L occur, the OpAmp must be able to drive the gate of Q2 and Q3 without slewing the transient. Therefore, the common source stage of the OpAmp must provide a sufficiently large drain current, I_{D16}. The required I_{D16} can be reduced by choosing a lower W/L for transistors Q2 and Q3 to reduce the parasitic capacitance related to the gate. When designing the OpAmp for the slow loop there is a trade-off between the GBWP of the differential stage, the transistor dimensions of Q2 and Q3 and the necessary I_{D16} to reduce slewing.

Table 1 Device dimensions and drain current

Device	Width [μm]	Length [μm]	I_Q [μA]	g_m [μA/V]
Q1	4000	0.18	1.0000	6532
Q2,Q3	4	1	4.1280	43.980
Q4,Q5	30	1	4.1280	112.920
Q6	4	2	8.2560	89.780
Q7	1	2	2.0000	22.240
Q11,Q12	64	1	0.0157	0.445
Q13,Q14	2	8	0.0157	0.316
Q15	2	1	0.0315	0.855
Q16	64	1	1.0210	27.800
Q17	32	1	1.0210	23.460
Q18	64	1	1.0210	27.040

The design based on a slow and fast loop discussed above lead to the device dimensions, quiescent currents and transconductance presented in Table 1. The total quiescent current is 10.3 μA. A value of 4 pF was chosen for C_C.

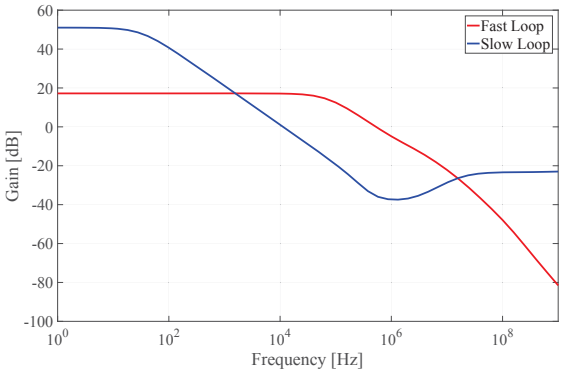

Fig. 3 Simulated open loop frequency response of the slow and fast loops, without extracted parasitics. $C_L = 0$

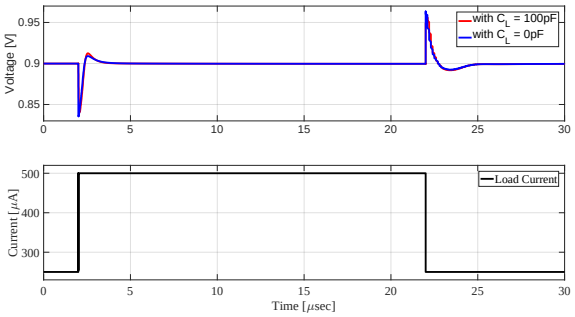

Fig. 4 Post layout transient response simulation of the complete circuit

3 Simulation Results

The proposed capacitor-free LDO linear voltage regulator has been implemented in a 180 nm CMOS process. The presented results are based on the post layout simulation. The bias current in the CS stage was 251 µA, when the load current is 250 µA. Current of 8.256 µA was distributed at the differential stage and 1.05 µA to the OpAmp, giving a total quiescent current consumption of 10.3 µA.

Post-layout simulation has been performed. Fig. 3 shows the open loop frequency response of the slow and fast loops at $C_L = 0$. The slow loop unity gain frequency is approximately two decades below that of the fast loop as we required. The PSRR is shown in Fig. 5, the value at 1 kHz with and without the load capacitor is 63 dB.

The design of intended for hearing aids, in such applications two audio channel are used, one of channels is continuously turned on and therefore a constant DC output current of 250 µA is needed. When needed to power up the other channel another 250 µA are required therefore the load step was set

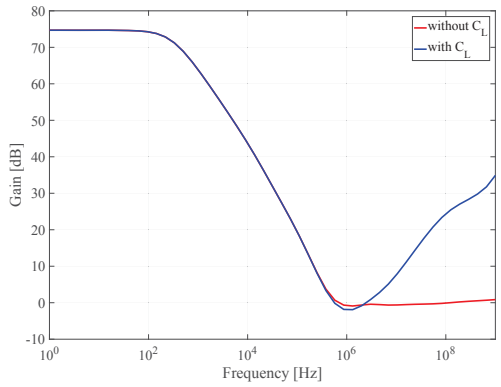

Fig. 5 Power Supply Rejection Ratio

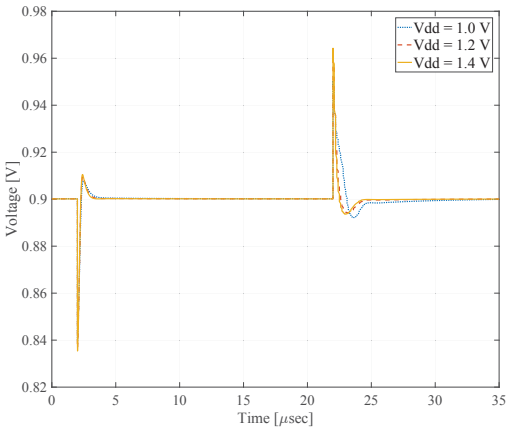

Fig. 6 Transient response simulation of the complete circuit with different supply voltages

from 250 - 500 µA. The transient response of the capacitor-free LDO voltage regulator for a current step of 250 - 500 µA with a rise and fall time of 1 ns is shown in Fig. 4. The simulation was preformed with and without C_L. ΔV_{out} without a load capacitance is 64 mV, while for $C_L = 100$ pF the spikes reach 56 mV. It should be noted that a smaller current step or longer rise time will decrease the spikes. Fig. 6 presents the transient analysis with different voltage supplies.

4 Experimental Results

The layout is presented in Fig. 7 shows the chip image with the proposed regulator layout. The LDO has been designed with measures 174 µm x 68 µm which occupies an area of approximately 0.012 mm^2. Common centroid matching and dummy devices have been used. The pass transistor Q1, differ-

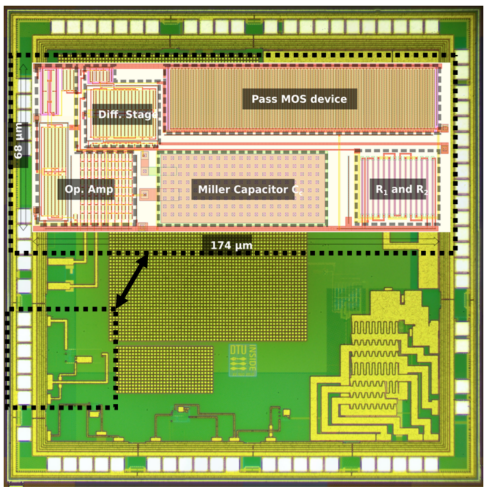

Fig. 7 Chip image with the layout of the proposed LDO linear regulator

ential stage, op-amp stage, resistors and the compensating capacitor can be seen in the layout figure. Most of the area is consumed by the power transistor and the Miller compensation capacitor.

An external reference voltage V_{ref} of 0.6 V and resistors $R_{L1} = 3.6\ k\Omega$ and $R_{L2} = 3.6\ k\Omega$ were used to imitate the DC load current and step. This set-up can be seen in Fig. 8. To verify the operation of the proposed regulator, a load current step from 250 - 500 µA with a rise and fall time of 1.5 µs was applied to the LDO with and without the load capacitor. The current step was implemented using the resistor R_{L2} and NMOS transistor with a signal generator connected to the gate to create the step from 0 - 250 µA. While R_{L1} is used to set the DC output current to 250 µA. The load step was not implemented on-chip, this caused a measurement limitation setting the current step edge time to the required 1 ns.

The transient response of the proposed design showed a maximum overshoot and undershoot of 26 mV and 26 mV with settling time of 3.5 µs and 1.5

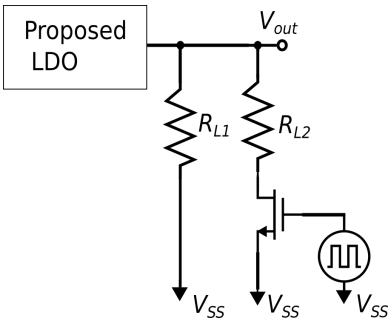

Fig. 8 Setup for LDO measurements

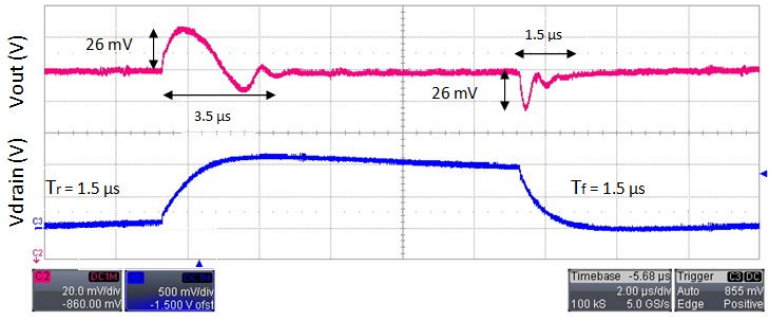

Fig. 9 Measured load transient response of the proposed LDO regulator without load capacitor

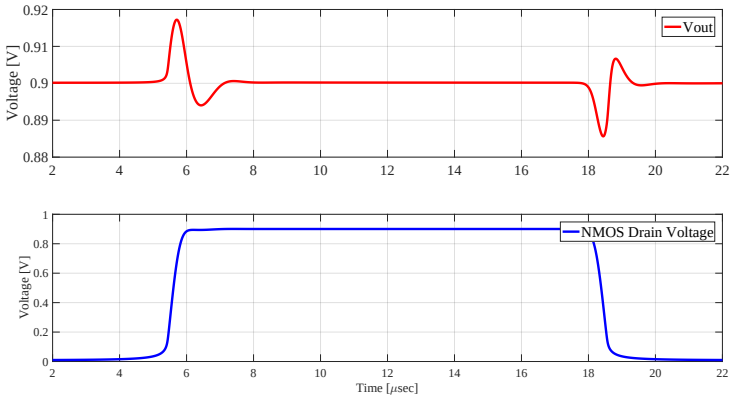

Fig. 10 Post layout transient response simulation of the proposed LDO regulator without load capacitor and with edge time 1.5 µs

µs respectively, shown in Fig. 9. The transient response with a load capacitor was similar to Fig. 9 and therefore is not presented. The quiescent current is 10.5 µA as expected like in the simulations. The circuit is intended to operate with an on-chip load as described in the simulation section, the edge time simulated was 1 ns. With the measurement setup we could not produce such a steep current step. The experimental current step rise and fall time were set to 1.5 µs and compared with the simulation results with same edge time. We assume that the correlation between the simulation and measurements results with rise/fall time of 1.5 µs can also be applied when the edge time is set to 1 ns.

The simulation results with rise and fall time of 1.5 µs are shown in Fig. 10. The simulation overshoot and undershoot is 18 mV and the settling time is equal to 3 µs. The simulation and measurements are quite compatible but not identical due to uncompleted model like the NMOS transistor for the setup and other phenomenons.

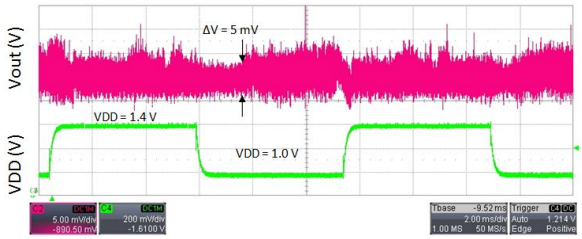

Fig. 11 Measured line transient response of the proposed LDO regulator

The measured line transient response of the proposed LDO without the use of an output capacitor is shown in Fig. 11. VDD varying from 1.0 V to 1.4 V, with rise and fall time 0.3 ms. The results include noise, we can conclude that the line regulation is smaller than $\frac{5mV}{0.4} = 12.5$ mV/V.

5 Performance Comparison

The presented theory and results of the proposed LDO linear voltage regulator show that external capacitor can be replaced by the design proposed. This design is suitable to supply low current to internal circuitry like needed in hearing aids. The design is simple to implement, with small area, which makes it ideal for a system-on chip. Simulations show good performance when compared with known capacitor-free topologies. For the purpose of comparison with other regulators we define a figure of merit (FoM) from [4]. This is used for standardized comparison in capacitor-free regulators as in the table. For this parameter, the smaller the FoM, the better the transient response of the regulator.

$$FoM = K\frac{\Delta V_{OUT,pp} I_Q}{\Delta I_{out}} \tag{9}$$

Where, $\Delta V_{OUT,pp}$ is the sum of the undershoot and overshoot and K is the edge time ratio which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{smallest } \Delta t \text{ among the designs for comparison}} \tag{10}$$

The unit of the FoM is volt as noted in Table 2. The K factor depends on the designs considered for comparison, because the edge time of our simulation work is the smallest, it K factor is equal to 1 while for the measurements results the edge time of 1.5 µs will result in $K = 1500$.

The performance comparison between the proposed design and some selected published LDOs is shown in Table 2. The FoM of the proposed design when comparing to similar designs is the second lowest for the simulation results. For the measurements the FoM is quite high as a result of the large

Table 2 Comparison of existing work

	Units	[1]	[2]	[5]	[3]	[4]	[8]	[9]	[6]	[10]*	This Work A**	This Work B***
Year		2003	2007	2009	2010	2010	2013	2015	2016	2016	2017	2017
Technology	[μm]	0.6	0.35	0.35	0.35	0.09	0.11	0.18	0.5	0.18	0.18	0.18
V_{in}	[V]	1.5 - 4.5	3.0 - 4.2	1.8 - 4.5	0.95 - 1.4	0.75 - 1.2	1.8 - 3.8	1.4 - 1.8	2.3 - 5.5	1.0 - 1.4	1.0 - 1.4	1.0 - 1.4
V_{out}	[V]	1.3	2.8	1.6	0.7 - 1.2	0.5 - 1	1.2	1.2	1.2 - 5.4	0.9	0.9	0.9
I_{out}(max)	[mA]	100	50	100	100	100	200	100	150	0.5	0.5	0.5
$I_{quiescent}$	[μA]	38	65	20	43	8	41.5	141	40	10.3	260.5	10.5
$V_{dropout}$	[mV]	200	200	200	200	200	200	200	100	100	100	100
Undershoot	[mV]	120	90	78	70	73	385	110	96	64	26	26
Overshoot	[mV]	90	90	97	70	114	200	85	120	64	26	26
$\Delta V_{OUT,pp}$	[mV]	210	180	175	140	187	585	195	216	128	52	52
ΔI_{out}	[mA]	90	50	90	99	97	199.5	99.99	150	0.25	0.25	0.25
Settling time	[μs]	2	15	9	3	5	0.65	30	3	3	3.5	3.5
Compensation cap	[pF]	12	21	7	6	7	3.2	9	29	4	4	4
$Cout$	[pF]	10000	100	100	100	50	40	100	470	100	100	100
PSRR @ 1 kHz	[dB]	-60	-57	N/A	N/A	N/A	N/A	N/A	-57	-63	-63	-63
Edge time ΔT	[μs]	0.5	1	1	1	0.1	0.5	1	1	0.001	1.5	1.5
Edge time ratio K		500	1000	1000	1000	100	500	1000	1000	1	1500	1500
FoM	[mV]	44.33	234.0	38.89	60.81	1.54	60.85	274.9	57.6	5.27	81276	3213
Active Area	[mm^2]	0.307	0.12	0.145	0.16	0.019	0.11	0.07	0.279	0.012	0.012	0.012

* Post layout simulation results of this work with the intended edge time of 1 ns
** Measurement results with an edge time of 1.5 μs, the constant DC output current of 250 μA was added to the quiescent current
*** Measurement results with an edge time of 1.5 μs

edge time from the setup limitations. Moreover, the DC output current of 250 μA (needed continuously to power one of the audio channel) decreases the FoM significantly when added to the quiescent current as can be seen in This Work A, Table 2. The column This Work B is the case when considering only the quiescent current of 10.5 μA without adding the intended static load of 250 μA, the improvement of the FoM is by a factor of 25. It should be noted that although the FoM is not ideal for comparing low power regulators it is still the most relevant FoM for capacitor-free LDOs, hence used in this paper. Our design has the smallest chip area, with the second lowest quiescent current of 10.5 μA while the load capacitance can be as large as 100 pF. Not only does the proposed regulator consume low power, but it provides a low dropout voltage and fast settling time.

6 Conclusion

We have demonstrated a new capacitor-free low-dropout linear regulator for hearing aids in 180-nm CMOS technology. The structure, post layout simulation, measurements and performance comparing have been provided. The proposed LDO with 0-100 pF load capacitance is stable throughout the load range without using any decoupling capacitor. The proposed regulator has proven a good transient performance. The internal compensating capacitor is as small as 4 pF and the chip total area is 0.012 mm^2. The LDO voltage regulator can operate with supply voltage between 1.0 - 1.4 V while having a quiescent current of 10.5 μA and small ΔV_{out} due to the two regulation loops. The achieved specification of the proposed LDO makes it suitable for hearing aids and similar SoC applications.

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